REMARKS

The present application was filed on July 23, 2001 with claims 1-29. Claims 1 and 18-29 were canceled and claims 30 and 31 were added. Claims 2-17, 30 and 31 are pending in the application. In the outstanding Office Action dated April 7, 2004, the Examine rejected claims 2-17, 30 and 31 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,225,674 to Lim et al. (hereinafter "Lim"), in view of U.S. Patent No. 5,631,572 to Sheen et al. (hereinafter "Sheen").

In response to the present Office Action, Applicant traverses the §103(a) rejection for at least the reasons set forth below. Applicant respectfully requests reconsideration of the present application in view of the following remarks.

Claims 2-17, 30 and 31 stand rejected under §103(a) as being unpatentable over the combination of Lim and Sheen. With regard to independent claims 3, 30 and 31, the Examiner acknowledges that Lim fails to teach an integrated circuit including a conductive layer comprising "a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net" (present Office Action; page 2, last paragraph; page 3, last paragraph; page 7, first paragraph). However, the Examiner contends that Sheen discloses such a feature. Applicant respectfully disagrees with this contention.

With regard to independent claims 3, 30 and 31, Applicant submits that the Examiner fails to establish a *prima facie* case of obviousness. "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation . . . to modify the reference or combine reference teachings. Second, there must be some reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations" MPEP §706.02(j). While it is sufficient to show that a *prima facie* case of obviousness has not been established by showing that only one of the above requirements has not been met, Applicant respectfully asserts that none of the requirements have been met.

Applicant submits that independent claims 3, 30 and 31 are patentable over the prior art of record. First, there is no suggestion or motivation, either in the prior art references themselves or in the knowledge generally available to one skilled in the art, to combine or modify the teachings of Lim, which relates to semiconductor structures having isolation regions, in view of Sheen, which

relates to equipment for testing populated printed circuit boards for manufacturing defects. Lim and Sheen are directed to entirely nonanalogous fields of art, namely, semiconductor structures and printed circuit board testing, respectively. "Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination." *In Re Bond*, 910 F.2d 831, 833, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). "Particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed." *In re Kotzab*, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). The prior art of record provides no such teaching, suggestion, or incentive supporting the proposed combination of Lim and Sheen.

In this regard, the Examiner contends that "it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sheen et al. into the device taught by Lim et al. because it depends on the amount of noise that need be reduced" (Office Action; page 3, last paragraph to page 4, first paragraph). Applicant respectfully disagrees with this contention and asserts that Sheen fails to provide any mechanism whereby the noise may be reduced in the semiconductor device taught by Lim, thus further failing to provide the requisite motivation for combining the two references. Furthermore, the present invention is directed to "improving isolation in a mixed signal IC device by reducing a resistance of a buried layer in the IC device" (Specification; page 1, lines 5-6; emphasis added), which neither Lim nor Sheen are directed to.

For at least the above reasons, Applicant submits that there exists no suggestion or motivation to modify the references or combine reference teachings. Consequently, a *prima facie* case of obviousness has not been established.

Second, even assuming, *arguendo*, that Lim and Sheen can be combined, Applicant respectfully asserts that there is an absence of a reasonable probability of success in modifying Lim, as required in order to sustain a *prima facie* case of obviousness. Lim provides a semiconductor structure having shielding structures comprised of localized buried layers, while Sheen, in contrast, provides techniques for detecting defective connections on populated printed circuit boards. As

such, modification of Lim in view of Sheen is unlikely to result in any reasonable success in obtaining an integrated circuit configured in the manner claimed. Likewise, since Lim and Sheen are directed to entirely nonanalogous art, as set forth above, there exists no conceivable mechanism for modifying Lim in view of Sheen which would result in an integrated circuit including a conductive layer formed on a surface of the integrated circuit and operatively coupled to an isolation buried layer at a plurality of points spaced throughout the buried layer, the conductive layer including a plurality of conductive traces intersecting with and connecting to one another to form a net. For at least the above reasons, Applicant submits that there is an absence of a reasonable probability of success in modifying Lim in view of Sheen. Consequently, a *prima facie* case of obviousness has not been established.

Lastly, Applicant respectfully submits that, even assuming, *arguendo*, that a reasonable probability of success in modifying Lim in view of Sheen can be found, the prior art fails to teach or suggest all of the claim limitations. Specifically, Lim and Sheen, when considered either individually or in combination, fail to teach or suggest at least a conductive layer formed on a surface of an integrated circuit and operatively coupled to an isolation buried layer at a plurality of points spaced throughout the buried layer, the conductive layer including a plurality of conductive traces intersecting with and connecting to one another to form a net, as required by the subject claims.

As previously stated, the Examiner acknowledges that Lim fails to disclose an integrated circuit including a conductive layer comprising a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net. However, the Examiner contends that Sheen discloses this feature of the subject claims. Applicant respectfully disagrees with this contention and asserts that Sheen clearly fails to teach or suggest any integrated circuit having a conductive layer formed on a surface of the integrated circuit, and moreover fails to disclose a conductive layer configured in the claimed manner. In this regard, the Examiner contends that Sheen teaches such feature at column 10, lines 24-28, where it states that "selector 108 is configured to make connection to one net of conductive traces on PCB 100 and all IC leads connected to that network are tested by changing the control input to antenna selector 118."

Applicant respectfully disagrees with this contention.

While Sheen may disclose a "net of conductive traces," Applicant submits that such disclosure is not remotely analogous to the conductive layer formed on the integrated circuit, as set forth in the subject claims. First, the "net" taught by Sheen is formed on a printed circuit board, which is clearly not analogous to an integrated circuit as recited in claims 3, 30 and 31. Second, Sheen fails to disclose that the "net" comprises a plurality of conductive traces which intersect with and are connected to one another, as explicitly required by the subject claims. Accordingly, Sheen fails to supplement the deficiencies of Lim.

Since Lim fails to teach or suggest any reason to reduce the lateral resistance of the buried layer, Applicant asserts that it would not have been obvious to form a conductive layer on the surface of the integrated circuit in the manner claimed. In fact, forming a conductive net over the integrated circuit, as recited in claims 3, 30 and 31 of the present invention, may considerably reduce the circuit density of the integrated circuit. Therefore, absent a stated justification for doing so, which Lim and Sheen clearly fail to provide, it would be undesirable to modify Lim so as to form a conductive layer on the surface of the integrated circuit comprising a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net, as required by the subject claims.

With regard to claim 3, Applicant further submits that this claim requires that the conductive layer be coupled to the isolation buried layer "at a plurality of points spaced throughout the buried layer." Applicant reiterates the arguments set forth in the previous response dated April 16, 2003 that the Lim reference fails to teach or suggest this limitation. Rather, as shown in FIG. 2, Lim clearly discloses deep trenches (33 or 38) filed with P+ doped polysilicon material forming an isolation ring surrounding, and in electrical contact with, a periphery of the corresponding buried layer (12 or 13, respectively) (Lim; column 3, lines 62-64; column 4, lines 6-10). While Lim may disclose a silicide layer (112) "formed on the exposed portions of trench fill polysilicon 33 and 38" (Lim; column 8, lines 23-25), Lim fails to teach or suggest that the buried layer is coupled to a conductive layer on the upper surface of the integrated circuit at a plurality of points spaced throughout the buried layer, as required by the claimed invention.

Even assuming, *arguendo*, that the silicide layer (112) disclosed in Lim can be analogized to the conductive layer on the surface of the integrated circuit, and assuming further that the buried layer (12) in Lim is coupled to the conductive layer via the polysilicon isolation ring (33), Applicant submits that the isolation ring taught by Lim is only in electrical contact with, at most, an edge of the buried layer, and not coupled to the buried layer at multiple points spaced throughout the buried layer. Thus, a lateral (i.e., sheet) resistance across the buried layer, e.g., between a center and an edge of the buried layer, in Lim is not significantly reduced. Moreover, the ring structure connected along the edge (i.e., periphery) of the buried layer disclosed in Lim cannot, by definition, be connected to the buried layer at a plurality of points spaced throughout the buried layer, as required by the claimed invention.

For at least the foregoing reasons, Applicant asserts that the three basic criteria for establishing a *prima facie* case of obviousness have not been met. However, assuming, *arguendo*, that a *prima facie* case of obviousness can be sustained, Applicant respectfully submits that the prior art, when considered either individually or in combination, fails to teach or suggest at least a conductive layer including a plurality of conductive traces intersecting with and connecting to one another to form a net, as expressly set forth in claims 3, 30 and 31 of the present application. Accordingly, favorable reconsideration and allowance of claims 3, 30 and 31 are respectfully solicited.

With regard to claims 2 and 4-17, which depend from claim 30, Applicant submits that these claims are also patentable at least by virtue of their dependency from claim 30. Moreover, one or more of these claims define additional patentable subject matter in their own right. For example, claim 4 further defines the conductive net as including "a plurality of holes therein, at least a portion of the first circuit section being formed in one or more holes in the net." Likewise, claim 5 further defines the conductive net as overlaying at least a portion of the first circuit section. Applicant submits that these claimed features are not taught or suggested by the prior art of record.

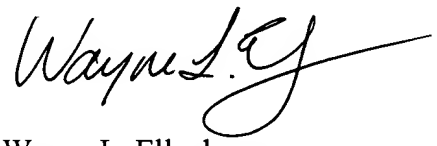
With regard to claims 4 and 5, the Examiner acknowledges that such features are not disclosed in Lim, but contends that the combination of Lim and Sheen discloses such features (present Office Action; page 4, paragraphs 2 and 3). Applicant respectfully disagrees with the

Examiner's contentions and submits that Sheen fails to teach or suggest a conductive layer formed on the surface of an integrated circuit and configured in the manner set forth in claims 3, 30 and 31, and furthermore fails to teach or suggest that a first circuit section of the integrated circuit is formed in one or more holes in the net (claim 4) or that the net overlays a portion of the first circuit section (claim 5). Furthermore, the Examiner fails to indicate with any specificity where in Sheen such features of claims 4 and 5 are disclosed.

For at least the reasons set forth above, Applicant submits that claims 2 and 4-17 are patentable over the prior art of record, not merely by virtue of their dependency from claim 1, but also in their own right. Accordingly, favorable reconsideration and allowance of claims 2 and 4-17 are respectfully solicited.

In view of the above, Applicant believes that claims 2-17, 30 and 31 are in condition for allowance, and respectfully request withdrawal of the §103(a) rejection.

Respectfully submitted,



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Wayne L. Ellenbogen
Attorney for Applicant(s)
Reg. No. 43,602
Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560
(516) 759-7662